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What is Claimed:

1. An semiconductor device, comprising:

a substrate having a source, a drain and a channel between said source and said drain; and

a gate structure disposed over said channel, said gate structure having a length of 1.25 μm or less and wherein the device does not include a lightly doped drain region.

2. A semiconductor device as recited in claim 1, wherein said length is in the range of approximately 0.25 μm to approximately 0.05 μm.

3. A semiconductor device as recited in claim 1, wherein said gate structure includes an oxide layer and said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

4. A semiconductor device as recited in claim 1, wherein a series source/drain resistance exists in the device, and said series source/drain resistance per μm of gate width is in the range of approximately 20 Ω to approximately 100 Ω.

5. A semiconductor device as recited in claim 1, wherein the device is an NMOSFET.

6. A semiconductor device are recited in claim 5, wherein said source and said drain are doped n+ and said substrate is p-type.

7. A semiconductor device as recited in claim 1, wherein said source and drain have a doping concentration in the range of approximately $1x10^{20}$ atoms/cm^3 to approximately $5X10^{20}$ atoms/cm^3.

8. A semiconductor device as recited in claim 1, wherein the device is PMOSFET.

9. A semiconductor device as recited in claim 8, wherein said source and said drain are doped p+ and said substrate is n-type.

10. A semiconductor device as recited in claim 2, wherein said oxide layer and said substrate form an interface and said interface is substantially planar and stress-free.

11. A semiconductor device as recited in claim 1, wherein said channel has a doping concentration of approximately $1X10^{16}/cm^3$ to approximately $1X10^{19}/cm^3$.

12. A field effect transistor, comprising:

a substrate having a source, a drain and a channel between said source and said drain;

a gate structure including an oxide, which forms and interface with said substrate, wherein said gate structure has a length in the range of approximately 0.05 μm to approximately 0.25 μm and the transistor does not include a lightly doped drain region.

13. A transistor as recited in claim 12, wherein said channel has a length in the range of approximately 0.05 μm to approximately 0.25 μm.

14. A transistor as recited in claim 12, wherein said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

15. A transistor as recited in claim 12, wherein a series source/drain resistance exists in the transistor, and said series source/drain resistance is in the range of approximately 20 Ω to approximately 100 Ω per μm of gate width.

16. A semiconductor device as recited in claim 12, wherein the device is an NMOSFET.

17. A semiconductor device as recited in claim 16, wherein said source and said drain are doped n+ and said substrate is p-type.

18. A semiconductor device as recited in claim 12, wherein said source and drain have a doping concentration in the range of approximately $1X10^{20}$ atoms/cm^3 to approximately $5X10^{20}$ atoms/cm^3.

19. A semiconductor device as recited in claim 12, wherein the device is PMOSFET.

20. A semiconductor device as recited in claim 19, wherein said source and said drain are doped p+ and said substrate is n-type.

21. A transistor as recited in claim 12, wherein said interface is substantially planar and stress-free.

22. A semiconductor device as recited in claim 12, wherein said channel has a doping concentration of approximately $1X10^{16}$/cm^3 to approximately $1X10^{19}$/cm^3.

23. A process for fabricating an integrated circuit, comprising:

forming a gate structure over a substrate, said gate structure having a length of approximately 1.25 μm or less; and

forming a source and a drain, said source and said drain not having lightly doped regions.

24. A process for fabricating an integrated circuit as recited in claim 23, wherein said process further comprises forming a channel before forming said source and said drain.

25. A process as recited in claim 23, wherein said forming said gate structure further comprises:

forming an oxide layer over said substrate; and

forming a conductive layer over said oxide layer.

26. A process as recited in claim 24, wherein said channel is doped by a halo implantation.

27. A process as recited in claim 23, wherein said length is in the range of approximately 0.25 μm to approximately 0.05 μm.

28. A process as recited in claim 25, wherein said oxide layer has a first oxide portion and a second oxide portion.

29. A process as recited in claim 23, wherein a spacer is not formed adjacent said gate structure.

30. A process as recited in claim 25, wherein said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

31. A process as recited in claim 23, wherein said source and said drain having doping levels in the range of approximately $1X10^{20}/cm^3$ to $5X10^{20}/cm^3$.

32. A process as recited in claim 24, wherein said channel has a doping level in the range of approximately $1X10^{16}/cm^3$ to approximately $1X10^{19}/cm^3$.

33. A process for fabricating an integrated circuit, comprising:

forming an oxide layer over a substrate;

forming a conductive layer over said oxide layer, said oxide layer and said conductive layer forming a gate having a length of 1.25 μm or less;

forming a channel in said substrate; and

forming a source and a drain, said source and said drain not having lightly doped regions.

34. A process as recited in claim 33, wherein said channel is doped by a halo implantation.

35. A process as recited in claim 33, wherein said length is in the range of approximately 0.25 μm to approximately 0.05 μm.

36. A process as recited in claim 33, wherein said oxide layer has a first oxide portion and a second oxide portion.

37. A process as recited in claim 33, wherein a spacer is not formed adjacent said gate structure.

38. A process as recited in claim 33, wherein said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

39. A process as recited in claim 33, wherein said source and said drain having doping levels in the range of approximately $1X10^{20}/cm^3$ to approximately $5X10^{20}/cm^3$.

40. A process as recited in claim 33, wherein said channel has a doping level in the range of approximately $1X10^{16}/cm^3$ to approximately $1X10^{19}/cm^3$.